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(54) Microprocessor-based unit memory testing system

(57) A method of and system for high-speed, high accuracy functional testing of memories in microprocessor-based units or boards under test includes a test system that is effectively permanently coupled to the unit-under-test bus structure during test execution and operates at the unit-under-test's clock rate.

A pseudo-random sequence of bits is written into a reference block of memory cells starting at the lowest address. The reference block is then replicated by iteretively reading the sequence and writing the bits into the successive blocks in a first direction until all the cells have been written to the highest address.

The reference block is then complimented and replicated over the complete range of addresses. Each cell is read from the highest address to the lowest address and complemented a second time. Then each cell is read for the lowest address to the highest address and compared with the pseudo-random sequence of bits to detect any difference therebetween.

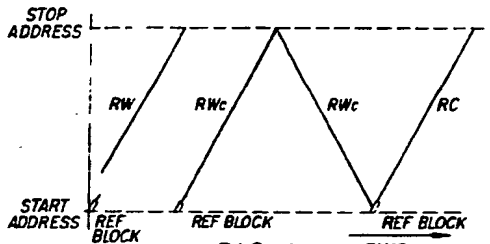

FIG. 4

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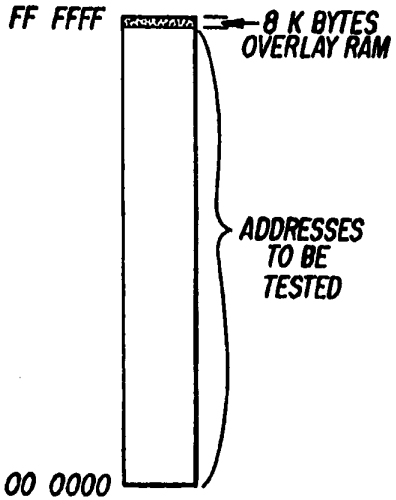

FIG. 2

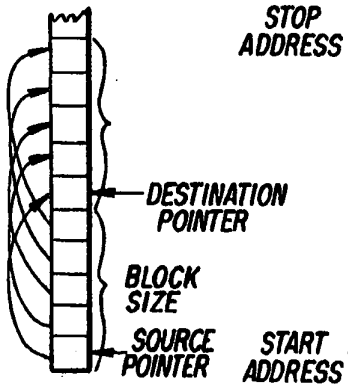

FIG. 3

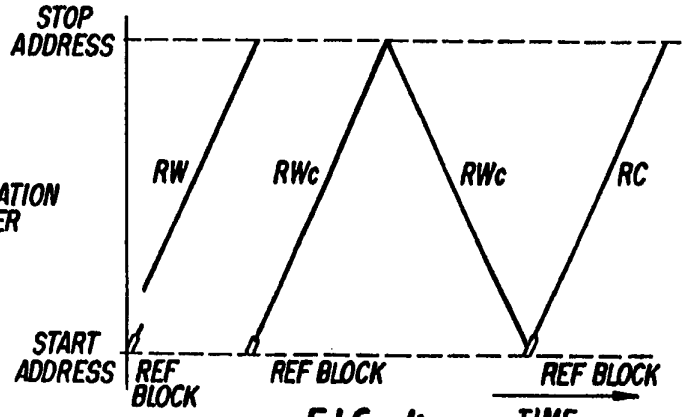

FIG. 4

units under test (UUTs) is typically limited by accuracy-versus-speed tradeoffs which are dependent upon the emulator architecture and the test algorithm used. The microprocessor emulation device, which contains a microprocessor of the same type as that of the UUT, connects directly or via an interface pod to the UUT's bus structure, for example, by connecting directly to the UUT's microprocessor socket. All testing performed by such emulation devices has heretofore been carried out in a bus-access mode wherein the emulation device makes single cycles of bus accesses and acts on each one before making another. That is, the emulation device knows which addresses to write and read, and for one bus cycle makes a connection to the UUT's bus with a specific address preloaded on it so that the UTT's memory either will be written at that address, or will give the value of the data stored at that address, depending on whether a write or a read command is given. Then the emulation device switches over to its internal circuitry to generate another write command with a new address, or deal with information read from the UUT's memory. With the aforementioned Jacobson algorithm, a new pseudorandom number is calculated for each address. Since the use of single cycles of bus accesses has been the basis for prior art RAM testing, whether resident in a mainframe or a pod, increases in memory size translate directly into more cycles of bus accesses and a corresponding increase in testing time. Thus, even with faster text algorithms such as Jacobson's 5N probabilistic functional RAM test procedure, the trend toward providing increased RAM space presents a problem in terms of the time it takes to test a UUT.

In accordance with one aspect of this invention, a method of and system for high-speed, high-accuracy functional testing of memories in microprocessor-based UUT's provides a new solution to the memory test speed-versus-accuracy problem which results in one to two orders of magnitude in speed increase while suffering very little, if any, decrease in accuracy.

According to one aspect of the present invention, a test system including a microprocessor of the same type as that of the UUT is efffectively permanently coupled to the bus structure of the UUT, and serves as a substitute microprocessor in executing a test program at a rate provided by the UUT's own clock to locate faults in the UUT memory.

pseudorandom bits is read by a first pointer and written into a next succeeding block by a second pointer. The pointers are moved together in spaced-apart relationship up through the memory in the first pass until all the cells are written. In the second pass, the pseudorandom bits in the reference block are complemented, and the read and write operations using pointers are repeated. The third and fourth passes are substantially the same as for the 5N test, except that the fourth pass involves two reads of each cell to compare bits indicated by the two pointers.

It is therefore one object of certain embodiments of the present invention to provide a method of and system for functional testing of memories in microprocessor-based units in which testing speed is increased by at least one or two orders of magnitude while maintaining high accuracy in identifying and reporting faults.

It is another object of certain embodiments of the present invention to provide a functional test algorithm which exploits block move and compare features of newer microprocessors.

It is a further object of certain embodiments of the present invention to provide a test system which is effectively permanently coupled to the bus structure of a unit whose memory is being tested, and which executes memory test instructions at the unit's clock rate.

Other objects, features, and advantages of the present invention will become obvious to those having ordinary skill in the art upon a reading of the following detailed description given by way of example with reference to the accompanying drawings in which:-

FIG. 1 is a generalized block diagram of a test system in accordance with the present invention;

FIG. 2 depicts a memory map for use in overlaying a memory under test;

FIG. 3 shows an example of memory block movement wherein data can be moved from one range of memory addresses to another; and

FIG. 4 is a graph showing a RAM test algorithm in accordance with the present invention.

Referring to FIG. 1, a generalized block diagram of a test system for functional testing of memory devices in microprocessor-based units in accordance with the present invention includes a mainframe unit 10

interchangeable, and a user simply chooses one that is designed to interface with the particular type of microprocessor employed in the UUT. For this example, let us assume that the UUT's microprocessor is the aforementioned 80286, and accordingly the interface pod 12 includes a complete 80286 kernel including microprocessor (uP) 42, RAM 44, ROM 46, and the earlier mentioned I/O interface 40 interconnected by data and address buses 48 and 50, respectively. Connected to the data and address buses 48 and 50 are data and address buffers 54. The data buffers are bidirectional and are enabled by a control signal from a timing and control circuit 56. The address buffers are output-only buffers. Interposed between the data/address buffers 54 and the microprocessor connector 16 is a protection circuit and logic-level-sensing network 58 that protect the interface pod 12 circuitry from over-voltage conditions and contain source and sense resistors to detect output drivability faults. For this particular interface pod, the microprocessor inputs from the UUT are referred to as status lines, and outputs to the UUT are referred to as control lines.

The mainframe unit 10 and interface pod 12 as herein established are largely conventional; however, the structure is set forth to provide a complete understanding of the novel memory testing mode of operation to be described. In normal mode of operation, typically called the troubleshooting mode, the mainframe/pod operation is substantially as described in U.S. Patent No. 4,455,654.

The operating mode of interest is a second, or ancillary mode referred to as "RUN UUT" wherein the interface pod microprocessor 42 is effectively permanently connected through its buffers to the UUT's bus structure 22 to serve as a substitute microprocessor in executing the UUT's own internal programs such as those contained in ROM 26. In this mode of operation, the interface pod 12 adopts such microprocessor functions as those associated with the status/control lines, interrupt handling, timing, and memory and I/O addressing. Also, and perhaps most significant, microprocessor 42 executes the programs at the rate provided by UUT clock 28.

In order to effect functional testing of the UUT memory, i.e., RAM 24, memory test instructions or programs may be stored in and executed from the UUT's executable memory, or, preferably, such memory test

In memory test systems not having overlay memory capability the speed advantage of the present invention can still be attained by first positioning and testing a large enough portion of the UUT RAM to contain the memory test program by using the prior art bus access technique, then loading the memory test program into the tested portion of the UUT RAM to test the remainder of the UUT RAM using the present invention. Overlay memory, however, offers somewhat higher confidence in test results since the electrical integrity of interface pod 12 is typically regarded as better than that of a suspect UUT memory device.

Another feature of the present invention that results in an increase in memory testing speed is the use of block- or string-orientated instructions specific to the emulated processor to perform DMA-like memory transfers without suffering the overhead of multiple instruction fetches and executions for each memory address tested. Newer microprocessors such as the 80286 have block move and compare features, which permit moving and comparing large blocks of data from ranges of addresses. For example, the 80286 is capable of moving up to 64 kilobytes of data with a single block move instruction. Thus, rather than using a memory test program instruction that accesses data from a single address, data from a range of addresses may be accessed.

Referring to FIG. 3, a simple example of block movement is shown. A source pointer indicates the first address in a block which for this example has five addresses. Data is written into the five addresses. A destination pointer indicates the first address of a five-address block into which data is to be moved. While the very next address, i.e., "6" is indicated by the destination pointer, in actuality any desired address could be indicated. Upon command, the data in address "1" through "5" are moved to addresses "6" through "10" respectively, as shown by the arrows in FIG. 3. Thus, particularly for microprocessor-based boards or units having large memories, exploitation of block move and compare operations provide for another order of magnitude speed increase of memory tests.

A memory test algorithm which takes advantage of the block move and compare operations in accordance with one aspect of the present invention is represented schematically in FIG. 4. The algorithm comprises four sweeps or passes of the RAM addresses, performing three

the UUT RAM and the first location following the bit-wise complemented pseudorandom data so that data can be read from the address designated by the source pointer and written to the address designated by the destination pointer. And as before for the first pass of the memory, a string move operation is performed, this time filling the UUT RAM with a series of complemented blocks of data. At this point, every data cell has made at least one transition in value, e.g., from zero to one or one to zero.

Next, a downward sweep from the highest address to the lowest address is performed. At each location, data is read, compared with its expected value, complemented, and written back. If any location returns a value which does not match the expected data, the test halts and the erroneous results are noted. By the time the lowest address is processed, all data cells have transitioned through both logic states.

For the fourth and final pass through the memory, data at the low-address end of the UUT RAM is read and compared with the original pseudorandom data. Next, the remaining memory locations are read and compared to their expected values. Again, this can be accomplished for the 5N algorithm using the source pointer to repetitively read the reference block while the destination pointer sweeps up through the address range of the memory reading and comparing the data, and, in the case of an 8N algorithm, an upward sweep through the memory is initiated with pointers set up to perform a string compare between locations which have already been validated and locations one block length higher in memory. Again, if any location does not return the expected data value, the test halts, and erroneous results are noted.

The above-described functional test algorithm may be written as a set of instructions to be stored in and executed from UUT 20's executable memory, or stored in and executed from overlaid memory located in interface pod 12 as described earlier. The block of pseudorandom data may be provided by a pseudorandom generator located either in interface pod 12 or in mainframe unit 10. Note that the pseudorandom data for the entire test need be calculated only once, and that the original data is re-used and manipulated where appropriate. The block of pseudorandom data may be stored in the overlay RAM and copied to the reference block area at the low-address end of the UUT RAM. Also,

CLAIMS

1. A method of functionally testing a memory having a plurality of addressable cells, comprising the steps of:

(a) writing a pseudorandom sequence of bits into a predetermined number of consecutively-addressed memory cells to provide a reference block:

(b) replicating said reference block by iteratively reading said pseudorandom sequence of bits and writing said bits into next successive blocks in a first direction until all of the memory cells are written;

(c) complementing the contents of said reference block;

(d) again replicating said reference block by iteratively reading complemented bits and writing said complemented bits into next successive blocks in said first direction until all of the memory cells are written;

(e) sequentially reading each cell in a second direction opposite said first direction, complementing the data therein, and writing said complemented data back into said cell;

(f) again reading each cell in said first direction and comparing said complemented data with said pseudorandom sequence of bits to detect differences, and, in response,

(g) identifying any memory faults.

2. A method in accordance with claim 1 further comprising the step of comparing data read from each cell in step (e) with an expected value to detect differences, and, in response, identifying any memory faults.

3. A method in accordance with claim 1 wherein the number of memory cells in said reference block is relatively prime with respect to mathematical powers of two.

4. A method in accordance with claim 1 wherein the replicating in steps (b) and (d) is accomplished in conjunction with a first pointer to indicate the cell being read and a second pointer indicating a cell being written.

5. A method in accordance with claim 4 wherein said first and second pointers are controlled by block move instructions from an associated processor.

(b) complementing all of the bits in said plurality of addressable cells by first complementing the bits in said reference block and replicating said reference block over said range to the high address;

(c) sequentially reading each cell over the range from the high address to the low address, and complementing the bit in each cell a second time to restore a logic state first written in step (a); and

(d) sequentially reading each cell over the range from the low address to the high address, and comparing the second-complemented bit in each cell with said pseudorandom sequence of bits to detect any differences therebetween.

12. A method in accordance with claim 11 further comprising the step of indicating any memory faults in response to any detected differences.

13. A method in accordance with claim 11 further comprising the step of comparing the bit read from each cell in step (c) with an expect value to detect differences, and, in response, identifying any memory faults.

14. A method in accordance with claim 11 wherein said replicating in steps (a) and (b) is controlled by a microprocessor having block move capabilities.

15. A system for functionally testing a memory under test in which the memory under test is coupled to a bus structure in a microprocessor-based unit which also has a clock providing timing signals at a predetermined rate, comprising:

a test system microprocessor coupled to said bus structure for communication with said memory under test;

a test system memory associated with said test system microprocessor and coupled thereto, said test system memory containing a set of test instructions;

means for electrically transferring said set of test instructions to a portion of said memory under test; and means for coupling said timing signals to said test system microprocessor to cause said set of test instructions to be executed at said predetermined rate, wherein said test system microprocessor remains in direct communication with said memory under test while said set of test instructions are executed.

21. A method of functionally testing a memory substantially as hereinbefore described with reference to the accompanying drawings.

22. Test apparatus for functionally testing a memory substantially as hereinbefore described with reference to and as shown in the accompanying drawings.

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